Standard Three-Day Training Course on Space Electronics

Time	Day 1	Day 2	Day 3
09:00	**FPGA 1** Space-grade FPGA technologies, COTS vs. Qualified, CMOS Scaling	**Mixed Signal 1** Designing with ADCs : Understanding the ADC output spectrum	**Power 1** Power distribution: DC-DCs, linear and switching POLs
10:30	**Coffee**		
10:45	**FPGA 2** Space-grade SRAM, Flash & Antifuse FPGAs, fabrics, LUT vs. MUX, logic resources	**Mixed Signal 2** Designing with DACs : Understanding the DAC output spectrum RF ADCs/DACs, bandpass sampling, eliminating RF frequency conversion stages	**Power 2** Comparison of space-grade, isolated DC-DCs. SiC vs. GaN vs. Si Power Radiation Effects Power FETs, SEGR, SEB
12:15	**Lunch**		
13:30	**FPGA 3** Radiation Effects Space-Grade FPGA Radiation Hardness, SEE Mitigation & Reliability	**Mixed Signal 3** System-level design: Clocking, jitter and powering ADC/DACs Analogue/RF front/back-end design	**Power 3** Comparison of space-grade, linear and switching POLs Identification of COTS
15:00	**Coffee**		
15:15 16:45	**FPGA 4** FPGA vendors' design flows and software & Comparison of space-grade FPGAs implementing spacecraft IP	**Mixed Signal 4** Comparison of space-grade ADC/DACs GSPS/MSPS/kSPS Identification of COTS	**Power 4** PCB stack design, layout, design-for-EMC, planes and analogue/digital partitioning. Post-layout simulation using Hyperlynx Analog and Boardsim
17:00	**Wrap Up**		