Fast, High-Capacity, Endurant MRAM for Space Applications

Real-time as well as Store & Forward on-board processing applications are increasingly requiring large amounts of fast, non-volatile memory. While space-grade NAND flash offers Gbs and Tbs of storage capacity, its speed, endurance, data retention together with the management of erroneous bits limits its use to missions with specific lifetimes and operational duty cycles. Magneto-resistive random-access memory (MRAM) offers the potential to provide GBs of fast, non-volatile storage without the above limits to enable the next generation of satellite applications.

Conventional SRAM stores each bit within a latch, typically realised using four or six transistors, and space-grade devices offer fast memory with capacities up to 32 Mb.

SDRAM stores each bit as a charge within a capacitor resulting in high-density devices with the latest space-qualified DDR4 offering capacities up to 48 Gb. The charge leaks requiring a constant power drain to periodically refresh the capacitors.

Both SRAM and SDRAM are volatile semiconductor technologies which use electron charge to store data. MRAM uses magnetic elements to store information, providing inherent radiation immunity, offering the speed of SRAM, a density approaching that of DRAM, the non-volatility of flash memory, unlimited read/write endurance and high-power efficiency at all times.

MRAM uses magnetic states and polarisation of a ferromagnetic material for writing data and magneto-resistance for reading back. Each storage element consists of a single transistor, magnetic tunnel junction (MTJ) memory cell as shown below. The MTJ comprises a fixed magnetic layer, a dielectric tunnel barrier and a free magnetic layer which can have its direction changed using a magnetic field or by applying a polarised current.

The insulating barrier is as thin as a few atomic layers and when an external bias is applied to the MTJ, electrons tunnel through the normally insulating material changing its resistance. A logical zero is stored when both layers have the same direction, *i.e.* the MTJ has low resistance, and a logic one when both layers have different directions, *i.e.* a high resistance.

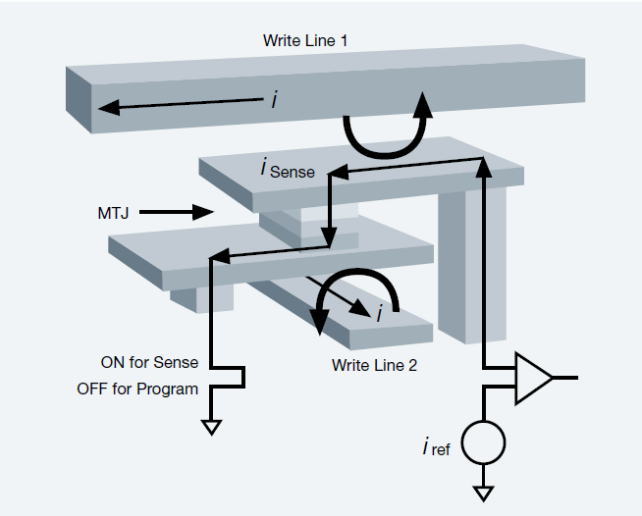

Figure 1 : Schematic of a single transistor, MTJ cell [Freescale].

Data is stored as a magnetic state rather than a charge and sensed by measuring its resistance without disturbing its polarization. This offers a number of major benefits for space applications:

1. The magnetic state does not leak away with time so your information remains when power is turned off.

2. Switching between the two states does not involve the actual movement of electrons or atoms, thus no wear-out mechanism exists.

3. MRAM is immune to bit flips (SEUs) due to radiation effects, latch-up resistant up to 85.4 MeV/cm^2/mg and a measured total-dose tolerance up to 1 Mrad(Si). Additional RHBD practices are required for support circuitry at a device level which differ by vendor, impacting actual radiation hardness.

4. Data retention of 10 years at +125°C and up to 1,000 years at +85°C.

Today, the fabrication of a MTJ has been integrated within the standard CMOS process enabling the economic production of parts. With conventional flash memory, endurance specifies the maximum number of program cycles without unrecoverable errors. Every erase operation introduces a defect in the oxide of a memory's cell structure which accumulate over time, defining the product's end-of-life. At some point, wear-out-induced errors prevent a flash cell from operating normally, rendering it unusable. MRAM does not store charge and uses magnetic states for storage: programming is achieved by pulsing a current through an MTJ, causing the magnetic polarisation to switch (up/down) by the Spin Transfer Torque effect. Reading is achieved by sensing different MTJ resistance states. The endurance of flash memory can be specified as 10^5 and MRAM as 10^{16} with certain implementations having a non-destructive read, embedded error correction and other techniques to bolster reliability.

MRAM offers the speed of SRAM, a density approaching DRAM, the non-volatility of flash memory, unlimited read/write endurance and low power consumption. It is ideal for real-time, on-board processing requiring non-volatile look-up tables and coefficients, in-orbit Edge computing, booting space-grade SRAM-based FPGAs and storing multiple configuration images. In fact, for these reasons, certain recent MRAM generations provide viable options for unified memory architectures, enabling design simplification, SWAP-C optimization at the design stage, but also with downstream impact to test and qualification.

Avalanche Technologies offers a range of rad-hard MRAM solutions for space applications based on their proprietary, two-transistor perpendicular MTJ (pMTJ) with capacities from 1 to 8 Gb with either 16/32-bit parallel or serial (Dual QSPI) interfaces. By the end of 2022, the company expects to add 16Gb DDR3 options to be leveraged as Persistent DRAM.

Development kits can be requested from the Avalanche website, IBIS and Verilog models are available and a NASA paper summarising radiation testing can also be downloaded. Within Europe, rad-tolerant parts are procured through Protec Semiconductor and in North America from Falcon Electronics. Radiation reports for the latest generation of devices are available upon request with a signed NDA.

Avalanche's latest (Gen. 3) parallel-interface devices are offered up to 4 Gb, packaged in a 15 x 17 mm, 142-ball FBGA specified from -40 to +125°C. D-QSPI parts are also available up to 8 Gb in an 88-ball FBGA in the same temperature range. The 1 Gb part is shown below:

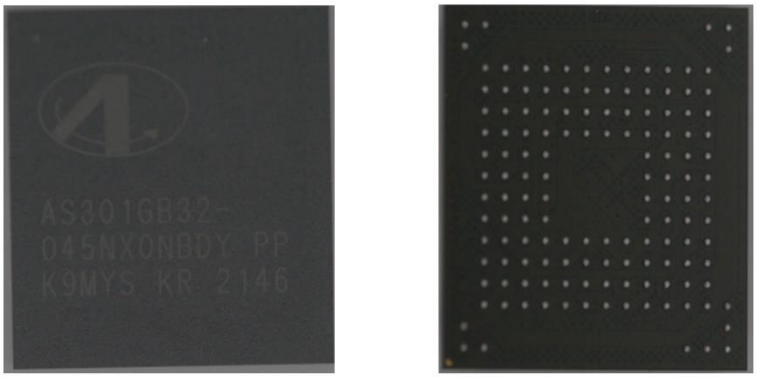

Figure 2 : Gen. 3, 32-bit parallel-interface, 1 Gb MRAM part.

3V3/1V8 Gen. 2, 16-bit parallel parts offering capacities up 64 Mb are available in a 10 x 10 mm, 48-ball FBGA specified from -40 to +125°C. Serial QSPI devices are also available up to 16 Mb in a 5.28 x 5.23 mm, 8-pin SOIC.

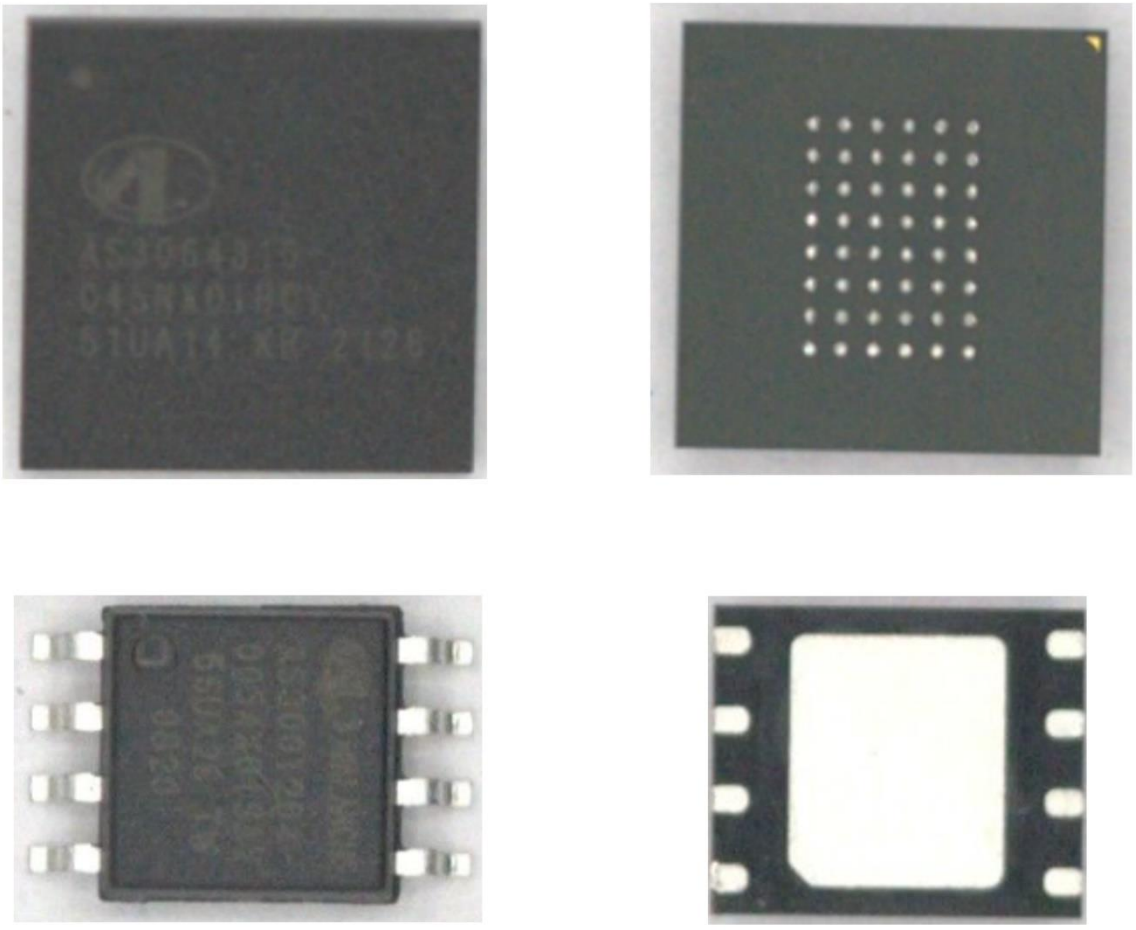

Figure 3 : Gen. 2, serial-Interface MRAM parts.

Space Grade devices offered by Avalanche Technology come in a high-temperature plastic package using a JEDEC flow plus 48-hour burn in, but additional options for extended temperature, packaging (die, hermetic, etc.) and qualification flow are offered through providers such as Micross.

Until next month, the first person to tell me why MRAM is a low-power memory technology will win a Courses for Rocket Scientists World Tour tee-shirt. Congratulations to Dae-Seong from South Korea, the first to answer the riddle from my previous post.

Dr. Rajan Bedi is the CEO and founder of Spacechips, which designs and builds a range of advanced, L to Ku-band, ultra high-throughput transponders, on-board processors and Edge-based OBCs and for telecommunication, Earth-Observation, navigation, internet and M2M/IoT satellites. The company also offers Space-Electronics Design-Consultancy, Technical-Marketing, Business-Intelligence, Avionics Testing and Training Services. (www.spacechips.co.uk). Rajan can also be contacted on Twitter or Linked-In to discuss your space-electronics' needs, https://twitter.com/DrRajanBedi and https://www.linkedin.com/in/drrajanbedi/.

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